We claim:

1. A method of forming a metal interconnect in an opening formed on a substrate, comprising:

(a) providing a substrate with an opening formed therein, said opening has sidewalls, a top, and a bottom;

(b) forming a seed layer within said opening;

(c) forming a first metal layer on said seed layer by a first electrochemical plating (ECP) process to partially fill said opening;

(d) performing a first anneal step;

(e) forming a second metal layer on said first metal layer with a second ECP process to fill said opening; and

(f) performing a second anneal step.

2. The method of claim **1** further comprised of a cleaning process between steps (c) and (d) and between steps (e) and (f).

3. The method of claim **1** further comprised of forming a diffusion barrier layer on the sidewalls and bottom of said opening prior to forming a seed layer.

4. The method of claim **3** wherein said diffusion barrier layer has a thickness of about 200 to 500 Angstroms and is comprised of one or more of Ta, TaN, Ti, TiN, TaSiN, W, and WN.

5. The method of claim **1** wherein said metal is copper and the seed layer is comprised of copper with a thickness between about 1000 and 2000 Angstroms.

6. The method of claim **1** wherein said first ECP process is performed at a temperature between about 10°C to 20°C and with a current density of about 5 to 15 mA/cm^2.

7. The method of claim **1** wherein said first and second anneal steps are performed in a process chamber at a temperature between about 180°C and 260°C for a period of about 10 to 200 seconds in a reducing gas or inert gas environment.

8. The method of claim **7** wherein the reducing gas is H_2 or NH_3.

9. The method of claim **1** wherein said first anneal step is performed in a PECVD process chamber with a H_2 plasma treatment comprised of a H_2 flow rate between about 5 and 10 sccm, a RF power of about 200 to 400 Watts, a chamber pressure of about 0.1 to 10 Torr, and a chamber temperature from about 150°C to 350°C for a period of about 10 to 200 seconds.

10. The method of claim **1** wherein said second anneal step is performed in a PECVD process chamber with a H_2 plasma treatment comprised of a H_2 flow rate between about 1 and 10 sccm, a RF power of about 300 to 400 Watts, a chamber pressure of about 0.1 to 10 mTorr, and a chamber temperature from about 150°C to 400°C for a period of about 10 to 200 seconds.

11. The method of claim **1** wherein the second ECP process is comprised of a first deposition step having a current density of 20 to 60 mA/cm^2 and a second deposition step having a current density of about 60 to 100 mA/cm^2.

12. The method of claim **11** wherein said first deposition step has a current density of about 40 mA/cm^2 and is used to fill said opening and wherein the second deposition step has a current density of about 60 mA/cm^2 and overfills said opening.

13. The method of claim **1** further comprised of a CMP process following said second anneal wherein said second metal layer becomes coplanar with the top of the opening.

14. A method of forming a copper interconnect in an opening formed in a stack of dielectric layers on a substrate, comprising:

(a) providing a substrate with a stack of dielectric layers formed thereon;

(b) forming an opening comprised of a via and an overlying trench in said stack of dielectric layers, said via and trench each having sidewalls, a top, and a bottom;

(c) depositing a conformal diffusion barrier layer on the sidewalls and bottoms of said via and trench and depositing a seed layer on the diffusion barrier layer;

(d) depositing a first copper layer on the seed layer by a first electrochemical plating (ECP) process that fills said via and partially fills said trench;

(e) performing a first anneal step;

(f) depositing a second copper layer on said first copper layer with a second ECP process, said second copper layer fills said trench;

(g) performing a second anneal step; and

(h) planarizing said second copper layer to be coplanar with the top of the stack of dielectric layers.

15. The method of claim **14** further comprised of a cleaning process between steps (d) and (e) and between steps (f) and (g).

16. The method of claim **14** wherein said diffusion barrier layer has a thickness of about 200 to 500 Angstroms and is comprised of one or more of Ta, TaN, Ti, TiN, TaSiN, W, and WN.

17. The method of claim **14** wherein said seed layer is comprised of copper and has a thickness between about 1000 and 2000 Angstroms.

18. The method of claim **14** wherein the distance from the top of the trench to the bottom of the via is about 4000 to 13000 Angstroms.

19. The method of claim **14** wherein the first ECP process fills the via and about half of the trench.

20. The method of claim **14** wherein said first ECP process is performed at a temperature of about $10^{o}C$ to $20^{o}C$ and with a current density of about 5 to 15 mA/cm^2.

21. The method of claim **14** wherein the first and second ECP processes are performed in the same work piece and include an electrolyte solution comprised of $CuSO_4$, HCl, and one or more organic additives.

22. The method of claim **14** wherein said first and second anneal steps are performed in a process chamber at a temperature between about $180^{o}C$ and $260^{o}C$ for a period of about 10 to 200 seconds in a H_2, NH_3, or inert gas environment.

23. The method of claim **14** wherein said first anneal step is performed in a PECVD process chamber with a H_2 plasma treatment comprised of a H_2 flow rate between about 5 and 10 sccm, a RF power of about 200 to 400 Watts, a chamber pressure of about 0.1 to 10 Torr, and a chamber temperature from about $150^{o}C$ to $350^{o}C$ for a period of about 10 to 200 seconds.

24. The method of claim **14** wherein said second anneal step is performed in a PECVD process chamber with a H_2 plasma treatment comprised of a H_2 flow rate between about 1 and 10 sccm, a RF power of about 300 to 400 Watts, a chamber

pressure of about 0.1 to 10 mTorr, and a chamber temperature from about 150°C to 400°C for a period of about 10 to 200 seconds.

25. The method of claim **14** wherein the second ECP process is comprised of a first deposition step having a current density of 20 to 60 mA/cm^2 and a second deposition step having a current density of about 60 to 100 mA/cm^2.

26. The method of claim **25** wherein said first deposition step has a current density of about 40 mA/cm^2 and is used to fill the trench and wherein the second deposition step has a current density of about 60 mA/cm^2 and is used to overfill the trench.

27. The method of claim **14** wherein planarizing said second copper layer involves a chemical mechanical polish process.

28. The method of claim **14** further comprised of a third ECP process followed by a third anneal step after the second anneal step and before said planarizing step.

29. The method of claim **28** wherein the second ECP process is performed with a current density of about 40 mA/cm^2 and the third ECP process deposits a third copper layer on the second copper layer and is performed with a current density of about 60 mA/cm^2.

30. A method of forming a dual damascene structure, comprising:

(a) providing a substrate with a stack of dielectric layers formed thereon;

(b) forming an opening comprised of a via and an overlying trench in said stack of dielectric layers, said via and trench each having sidewalls, a top, and a bottom;

(c) depositing a conformal diffusion barrier layer on the sidewalls and bottoms of said via and trench and depositing a seed layer on the diffusion barrier layer;

(d) depositing a first copper layer by a first electrochemical plating (ECP) process that fills said via and partially fills said trench;

(e) performing a first anneal step;

(f) depositing a second copper layer on said first copper layer with a second ECP process, said second copper layer fills said trench;

(g) performing a second anneal step;

(h) depositing a third copper layer on said second copper layer with a third ECP process, said third copper layer overfills said trench; and

(i) performing a third anneal step.

31. A metal interconnect structure with a low concentration of impurities, comprising:

(a) a seed layer formed on the sidewalls and bottom of an opening comprised of a via and an overlying trench formed in a stack of dielectric layers on a substrate;

(b) a first metal layer on said seed layer that fills said via and partially fills said trench, said first metal layer has a first grain size, a first thickness on the sidewalls of the trench and a second thickness on the bottom of the trench; and

(c) a second metal layer on said first metal layer that fills said trench, said second metal layer has a second grain size and is coplanar with the top of said opening.

32. The metal interconnect structure of claim **31** wherein the metal is copper.

33. The metal interconnect structure of claim **32** wherein the seed layer is copper and has a thickness between about 1000 and 2000 Angstroms.

34. The metal interconnect structure of claim **31** wherein the distance from the top to the bottom of said opening is between about 4000 and 13000 Angstroms.

35. The metal interconnect structure of claim **31** wherein the impurities are C, S, and Cl and the carbon concentration is less than about 100 counts per second, the sulfur concentration is less than about 20 counts/sec., and the chloride concentration is less than about 10 counts/sec. as determined by a SIMS analysis.

36. The metal interconnect structure of claim **31** wherein the first grain size and the second grain size are about 1 micron.

37. The metal interconnect structure of claim **31** in which the seed layer, first metal layer, and second metal layer form a contiguous layer with no seam.

38. The metal interconnect structure of claim **31** wherein the metal interconnect has void defects of about 0.1 to 0.5 microns in size that number less than about 5 per substrate.

39. The metal interconnect structure of claim **31** wherein the metal interconnect has a resistivity of less than about 2.2 ohms-cm.